

BSc (H) Electronics II Year
Digital Electronics
Pre-University Exams08

Answer any **five** questions. **Q. 1 is compulsory.**

- 1) (a) IF 10111010 is a signed binary number, what is its decimal equivalent? (1)
(b) What is the terminal count of a 4 bit binary counter in the UP mode? In the DOWN mode? What is the next state after the terminal count in the DOWN mode? (1)
(c) Is the parallel load operation in a register synchronous or asynchronous? (1)
(d) What should be the JK inputs for a FF to act as a divide by 2 device? (1)
(e) An AND gate has 7 inputs. How many input words are in its truth table? What is the only input word that produces a 1 in its output? (1)
(f) Given a presettable 8 bit counter, what no. would you preset it to get a divide by 130 counter? (1)
(h) If $(648)_{10} = (x)_8$, find the value of (1)
(i) Find the Gray code of the binary no. 101101101 what is the significance of the Gray code? Where is it used? (2)
- 2) (a) Add 749_{10} to 183_{10} in BCD (2)
(b) $(355)_{10} = (x)_8 = (y)_{16}$ (2)
(c) Subtract 10011.11 from 1000001.0001 using 1's complement and 2's complement.
(d) Find the decimal equivalent of $(AE4)_{16}$ (1)
- 3) (a) Simplify the following Boolean Function together with don't care conditions using Quine McCluskey method (Tabulation Method)
$$F = \sum(1,3,13,15) + \sum_d(8,9,0,11)$$
 (4)
(b) A majority function is generated in a combinational circuit when the output is equal to 1 if the input variables have more 1's than 0's. The output is zero otherwise. (3)
- 4) (a) Design a counter with the following repeated binary sequence 1,3,4,6 using T FF's. (4)
(b) The input waveform to a JK FF is given below Assuming Q is initially low, sketch the output waveform when
(i) FF is + edge triggered
(ii) FF is M/S (3)
- 5) (a) The content of a 4 bit register is initially 1101. The register is shifted 6 times to the right with the serial I/P being 101101. What is the content of the register after each shift? (3)
(b) If the clock frequency to a 3 bit ripple counter is 4 KHz, What will be the frequency of the LSB? (1)
(c) Write the sequence of states for a 4 bit Johnson counter? (1)
(d) What is the modulus of a counter? If 2 counters with modulus m and n are cascaded what is the total modulus of the cascaded counter? (2)

- 6) (a) Design a synchronous Decade counter using J-K FF's by calculating the combination logics for J & K inputs. (4)
- (b) Define Set up time, Hold time (2)
- (c) Reduce the following

$$AB + A + AB \quad (1)$$