BSc (H) Electronics II Year
Digital Electronics
Pre-University Exams 07

M.M. 38 **Time 3 Hr**

Answer any **five** questions. **Q. 1 is compulsory.**

Q1. (a) IF 10111010 is a signed binary number, what is its decimal equivalent? (1)

(b) What is the terminal count of a 4 bit binary counter in the UP mode? In the DOWN mode? What is the next state after the terminal count in the DOWN mode? (1)

(c) Given a presettable 8 bit counter, what no. would you preset it to get a divide by 130 counters? (1)

(d) Which code is referred to as 'REFLECTIVE CODE'? Why? (1)

(e) Determine the value of x, y, z

$(x)_2 = (y)_8 = (z)_{10}$ ABH (2)

(f) What range of signed and unsigned values can be represented in 8 bits (2)

(g) Perform 2's complement subtraction on decimal numbers using 8 bits

$42_{10} - 90_{10}$ (2)

Q2. (a) A two seated airplane requires that both the pilot and the navigator have their seat belts tightened, before the plane can take off. However it is desired, that in case of solo flights, (without the navigator), the state of the navigator seat belt should not have any effect on the take off. Make the truth table and obtain the simplified logic expression foe system and design it using NAND gates. (4)

(b) Realize using 8:1 multiplexer

$Y(D,C,B,A) = \prod(1,4,6,9,10,11,14,15)$ (3)

Q3. (a) Design a sequential circuit with two D flip flops A & B and one input X. When X = 0, the state of the circuit remains the same. When X = 1 the circuit goes through the state of transitions from 00 to 01 to 11 to 10 back to 00 and repeats. (5)

(b) What is race around condition in JK flip flop? How is it overcome? (2)

Q4. (a) Find the simplified SOP form using Quine McCluskey method

$F(A,B,C,D) = \sum(1,4,6,7,9,10,15)$ (4)

(b) Design a free running oscillator to give a square wave output having a frequency of 20 KHz. The capacitance C should be kept at 100pF or greater. (2)

(c) In a Mod 64 synchronous counter, each flip flop has t_{pd} = 20ns and each AND gate has t_{pd} = 10ns. Find the maximum frequency of the counter. (1)

Q5.(a) It is desired to get an output frequency of 1.2 KHz from an input frequency of 18KHz. Draw a circuit of asynchronous counter for this purpose? (4)

(b) An 8 bit universal shift register contents are 11000110. What are the register contents after 2 right shifts, 3 left shifts and 1 right shift? D_{in} = 1. (2)

(c) In a 5 bit ripple counter, the input frequency is 8 MHz. What is the output frequency? (1)

Q6.(a) Indicate the flip flop for which the following statements apply:

(i) Has only one control input
(ii) Has two outputs which are complements of each other
(iii) Has an enable input instead of clock input
(iv) Has Set and Reset inputs but no clock input
(v) Will toggle on each clock pulse when its control inputs are both high
(vi) Is used to transfer data from one flip flop register to another. (3)

(b) How does two's complement adder/subtractor work? Explain with the help of the diagram? (2)

(c) Give the truth table of full subtractor (1)

(c) A 5 bit ripple counter starts at 0000. What will be the count after 144 input pulses? (1)